

DMC-110366

Synthesized 20 GHz Microwave Source Operation Manual

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Preliminary

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Information contained herein is preliminary, and subject to change without notice. Contact the author for comments or changes.

DMC-110366 Operation Manual

Introduction

The DMC-110366 is a phase-locked DRO (Dielectric Resonator Oscillator) synthesized frequency source with various models covering the frequency range of 19 GHz to 24 GHz, depending on the DRO resonator installed at the factory. Frequency stability is achieved through the use of an oven stabilized crystal oscillator. A second crystal oscillator and divider provides channel spacing in 17.5 MHz steps.

Output from the oscillator is provided by two SMA connectors, with each port supplying about +10dbm per port. Test points are provided for alarm (loss of lock or other malfunction) and monitoring of the PLL voltage.

Mechanical Description

The oscillator is housed in a machined metal housing. Provisions are made for mounting the unit to a baseplate with captive screws. A DIP switch for setting the final channel frequency is on top of the unit. A toggle switch, which is accessible through the top cover, disables the loop filter (test mode) and allows the DRO to free run. Also on or under the top cover is the frequency adjustment capacitor for the channel spacing (offset) oscillator.

External to the unit are SMA connectors for 20 GHz frequency output, offset frequency monitoring, power, alarm and PLL voltage monitoring. A screw cover on one end of the unit provides access to the inductor used to adjust the ovenized crystal frequency.

The microwave/RF portion is housed in a metal module embedded in one corner of the main housing. There are three circuit boards mounted in the main housing. The topmost board is the channel offset oscillator/divider chain, offset prescaler and divide by N counter. Below this, mounted upside down, is the oven oscillator/first multiplier chain. The bottom circuit board, also mounted upside down, contains the PLL, loop filter, alarm circuit and DC-DC converter.

Functional Description

An ovenized crystal overtone oscillator, running at about 105 MHz, provides the basic operating frequency and stability for the unit. The oven oscillator is followed by two doublers to give a basic reference frequency in the 420 MHz range. The 420 MHz signal is sent to the main RF unit (metal housing) through a PI matching network and multiplied into the 10 - 11 GHz range.

A voltage-tuned DRO oscillator running at 10 - 11 GHz is used as the basic microwave frequency-generating source. This is fed to a doubler, amplifiers and power splitter to provide two 20 GHz outputs at +10 dBm. A tuning screw in the top of the RF housing is used to tune the DRO. Turning the screw clockwise (in) raises the frequency of oscillation. The oscillator output (after doubling) is tuneable over a 1 GHz range. Be careful not to turn the tuning screw too far in, or damage to the DRO will result.

A sample of the 10 GHz DRO and the 10 GHz oven oscillator reference frequency are mixed together. The difference frequency is amplified and sent to a dual-modulus prescaler on the channel offset board. Output from the dual modulus prescaler is then sent to the divide by N counter PAL. The divide ratio for this counter is set by a nine-position DIP switch. The divide ratio is basically binary, except for the three LSB switches, which do not necessarily follow a binary sequence. The three LSB switches also control the divide by 10/11 function of the dual-modulus prescaler. The output from the divide by N counter is used as one input to the phase detector. The prescaler/divide by N circuit sets the difference frequency between the crystal reference and the DRO.

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A 14 MHz crystal oscillator is used as the channel offset reference. This is divided by 16 to supply a basic PLL reference frequency of 875 kHz. This is fed to the other input of the phase detector.

The phase detector outputs a voltage proportional to the difference between the channel offset reference frequency and the output of the prescaler/divide by N counter. The voltage is filtered and applied to the DRO tuning varicap input. The tuning voltage is steered so that the DRO frequency is equal to the crystal reference frequency plus the offset frequency set by the prescaler/divide by N counter.

An alarm circuit is used to detect loss of lock or loss of power output. The alarm output is an open collector transistor connected to an output pin. The output voltage swing of the PLL must be large enough to control the tuning varicap through its entire range. A DC-DC converter takes the 8.4 volt supply voltage and boosts it to about 20 volts, and is used to supply the PLL loop filter voltage drive to the varicap. A 7805 three terminal voltage regulator is used to supply +5 volts for the logic circuits.

Frequency Adjustment

Equipment required:

- Oscilloscope, DC to 200 MHz
- Frequency counter, 10 MHz to 26 GHz
- DC power supply, 8.4 volts at 1 amp
- SMA attenuator, 50 ohm, 10 dB, DC - 18 GHz
- SMA termination, 50 ohm
- A clean workbench (if you can find one)

Terminate one of the output ports with a 50 ohm terminator. Connect the 50 ohm, 10 dB pad to the other output port. This will protect the counter input and also provide a proper output load to the oscillator. Remove the top cover and the screw cover for the oven oscillator (located on one end of the unit). Connect the power supply to the voltage pins of the oscillator. Attach the negative lead to the ground lug (case or black wire) and the positive lead to the +8.4 volt pin (red wire).

Apply power to the unit and wait about 5 minutes for the crystal oven to stabilize. The current will be about 1 amp for about two minutes, then slowly drop to about 600 ma. Adjust the offset oscillator to 14.000000 MHz. This is accomplished by probing TTL IC US pin 12 or 13. You can use a fine point oscilloscope probe connected to the high-impedance input of the counter. Some oscilloscopes allow you to connect the counter to one of the oscilloscope channel amplifiers, so you can see the waveform and measure frequency at the same time. The frequency adjustment is located next to the 14 MHz crystal.

Ensure that the toggle switch is set to the "normal" position. Note the current setting of the DIP switches and the output frequency (in case you need to start the procedure from scratch). Now set switches 1 through 8 to the ON position, and set switch 9 to the off position. This should establish a base operating frequency. Fine frequency adjustment is accomplished by turning the oven oscillator tuning coil through the hole in the side of the unit. Now set the final operating frequency by setting the appropriate DIP switches. Monitor the PLL tuning voltage at the yellow wire test point. The voltage here should be about +10 volts. If it is significantly above or below this value, adjust the DRO tuning screw to center the tuning voltage at about +10 volts. Be careful not to turn the tuning screw too far in, or damage to the DRO will result. Recheck the output frequency, and adjust the oven oscillator tuning coil for the proper frequency if necessary. This is also a good time to check the frequency stability. When the final frequency setting is accomplished, remove power to the unit and replace the top cover and side cover screw.

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Miscellaneous Notes

Frequency stability is determined by:

- Quality of the 105 MHz crystal
- Quality of the 14 MHz crystal
- Power supply regulation

The power supply should be well regulated, since this unit is fairly sensitive to voltage fluctuations.

The crystal in the oven seems to be fairly stable; according to my preliminary testing, most of the units drift less than 5 to 10 Hz/second, and should be stable enough for SSB work. I haven't tried SSB operation yet on the bench, but I have listened to the CW signal with the setup shown in Fig. 3, and the signal seemed pretty clean with very little drift. Setting the PLL tuning voltage to midrange using the procedure in the previous section improves the stability quite a bit.

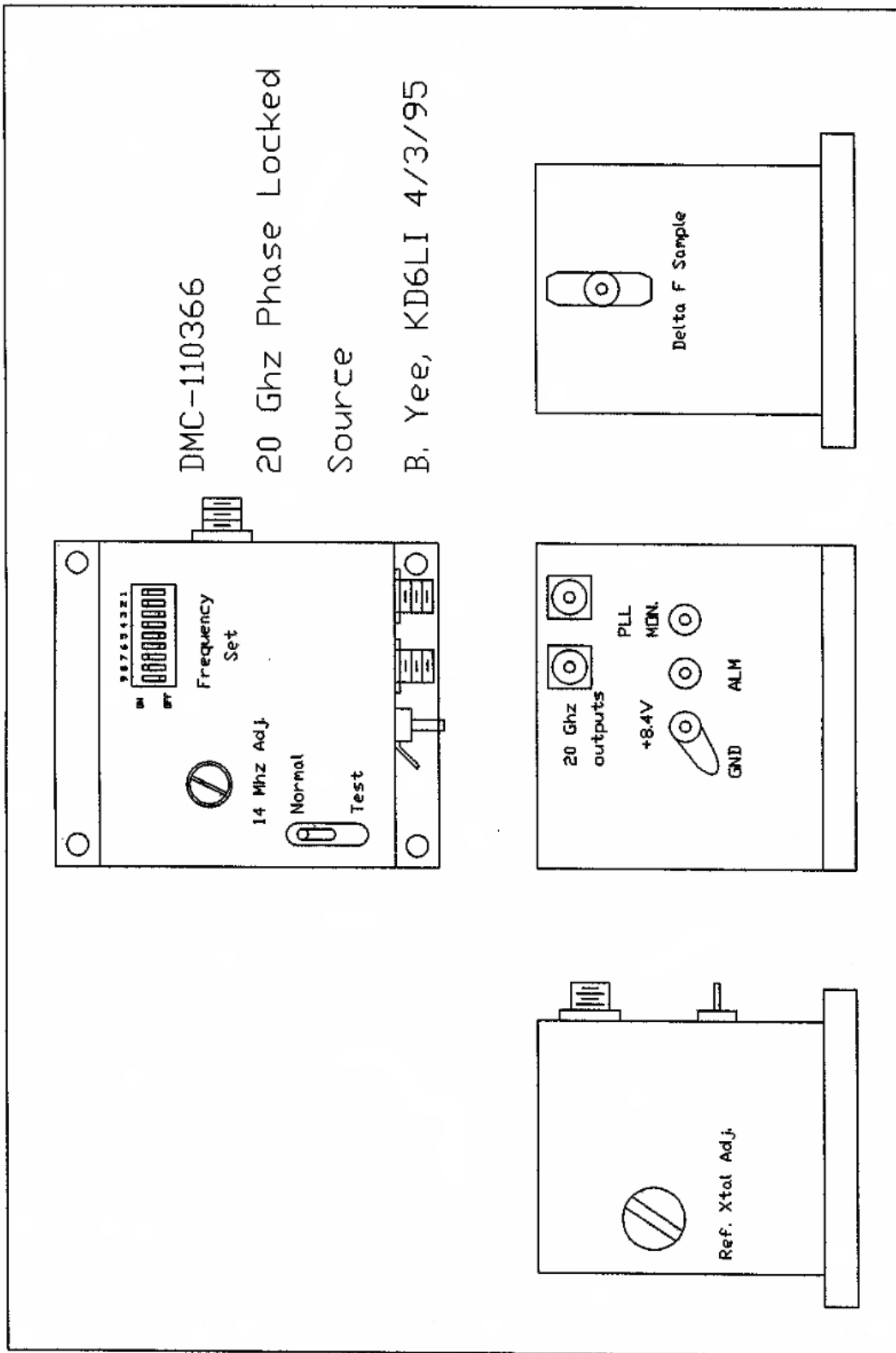
The 14 MHz oscillator seems to be stable enough, except that not being ovenized, it may tend to drift under field conditions. It should be possible to replace this with an external 10 MHz oven reference, which would give a PLL reference frequency of 625 kHz or 12.5 MHz channel spacing at 20 GHz.

It may be possible to change the oven oscillator crystal, although it is a somewhat risky procedure. Changing the crystal requires complete disassembly of the unit, with the exception of the 14 MHz channel offset oscillator board. The RF unit is normally plugged into sockets on the oven crystal board, but I have found on some units they are soldered on. Too much force used to separate them will result in the pins being ripped out of the RF unit.

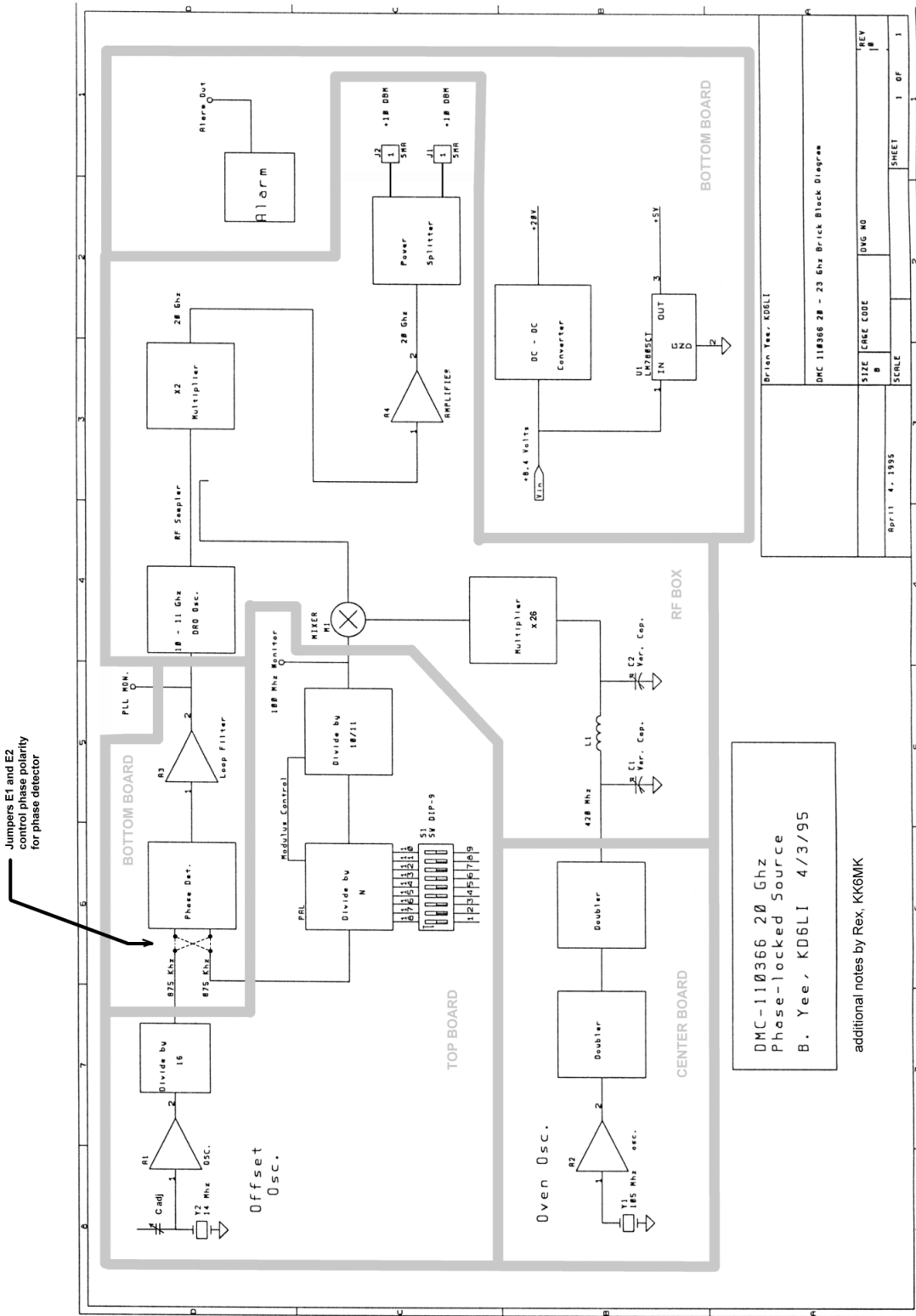
You may wish to stabilize the oven oscillator with a varicap scheme similar to that used by WA6CGR¹, or replace the crystal oscillator with an externally generated reference.

Bibliography

1. "A Universal Phase Lock Loop System for Microwave Use", Dave Glawson, WA6CGR, Proceedings of Microwave Update '94, Page 69, ARRL Publications



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Phase-locked Source
B. Yee, K06LI 4/3/95

additional notes by Rex, KKGMMK

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DMC 110366 20 - 20 Ghz Brick Block Diagram	
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April 4, 1995	1
SCALE	SHEET 1 of 1

DMC-110366
Evaluation Setup
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